CLAIMS:

What is claimed is:

1. An interface circuit for interfacing a system controller integrated circuit and a plurality of peripheral integrated circuits, said interface circuit comprising:

a node within said system controller integrated circuit commonly connected to a first and a second one of said plurality of peripheral integrated circuits;

first switch means for selectively connecting said node to a first circuit of the systems controller integrated circuit for communicating signals with reference to said first peripheral integrated circuit;

second switch means for selectively connecting said node to a second circuit of the systems controller integrated circuit for communicating signals with reference to said second peripheral integrated circuit;

signal means for early enabling and late disabling of said first and second switch means consistent with setup and hold times of the respective first and second peripheral integrated circuits.

2. The interface circuit of Claim 1, wherein said node is an output pin for providing an output signal to said first one and said second one of said plurality of peripheral integrated circuits, and wherein said first switch means comprises a selector within said system controller integrated circuit having a select input coupled to signal means.

3. The interface circuit of Claim 2, wherein said first peripheral integrated circuit is a memory device, said second peripheral integrated circuit is a bus controller, said first circuit is an address generator and said second circuit is a bus control generator.

4. The interface circuit of Claim 2, wherein said first circuit is a data signal generator and said second circuit is an address generator.

5. The interface circuit of Claim 2, wherein said first switch means comprises a tri-state buffer having an input coupled to said first circuit, an output coupled to said node, and an enable input coupled to said signal means; and wherein said second switch means comprises a second tri-state buffer having an input coupled to said second circuit, an output coupled to said mode, and an disable input coupled to said signal means.

6. The interface circuit of Claim 2, wherein said first and said second switch means comprise:

a multiplexer having inputs coupled to said first circuit and said second circuit and a select input coupled to said signal means; and

an output driver having an input coupled to an output of said multiplexer and an output coupled to said node.

7. The interface circuit of Claim 1, wherein said node is an input pin for receiving a first signal from said first peripheral integrated circuit and a second signal from said second peripheral integrated circuit.

8. The interface circuit of Claim 7 further comprising:

first chip select signal means coupled to said first peripheral integrated circuit for enabling communication with said first peripheral integrated circuit;

second chip select signal means coupled to said second peripheral integrated circuit for enabling communication with said second peripheral integrated circuit, and wherein said first circuit comprises a first transparent latch having a gate input coupled to said first chip select signal means, whereby a state of said node may be maintained at said first circuit when said signals means deselects communication said first peripheral integrated circuit, and wherein said second circuit comprises a second transparent latch having a gate input coupled to said second chip select signal means, whereby a state of said node may be maintained at said second circuit when said signal means deselects said second peripheral integrated circuit.

9. The interface circuit of Claim 1, wherein said node is a pin for receiving a first signal from said first peripheral integrated circuit and transmitting a second signal to said second peripheral integrated circuit, and wherein said second switch means comprises a tri-state buffer having an enable input coupled to said signal means an output coupled to said node and an input coupled to said first circuit.

10. The interface circuit of Claim 9, wherein said first circuit comprises a transparent latch having a gate input coupled to said signal means, whereby a state of said node may be maintained when said signal means disables said gate input.

11. The interface circuit of Claim 1, wherein said node is a bi-directional interface pin for interfacing bidirectional signals to said first and said second peripheral integrated circuits, wherein said first circuit and said second circuit include bidirectional input/output connections, wherein said first switch means comprises a transmission gate having a select input coupled to said signal means, a first terminal connected to said node and a second terminal coupled to said first circuit, and wherein said second switch means comprises a transmission gate having a select input coupled to said signal means, a first terminal connected to said node and a second terminal coupled to said second circuit.

12. A method for coupling a plurality of signals of differing types between a plurality of peripheral integrated circuits and a system controller integrated circuit, said method comprising:

generating a peripheral select signal within said system controller integrated circuit for early enabling and late disabling switch means consistent with setup and hold times of the peripheral integrated circuits;

generating a chip select signal from said peripheral select signal;

supplying said chip select signal to a corresponding peripheral integrated circuit chip select input;

selecting one of a plurality of internal signals each associated with one of said plurality of peripheral integrated circuits in conformity with said peripheral select signal; and

coupling said selected internal signal to an external pin connected to each of said plurality of peripheral integrated circuits, whereby said selecting and said coupling interface a internal signal associated with a peripheral integrated circuit corresponding to said chip select signal.